CONTINUE STEP 6
SECOND OF TWO WEEKS
This Week

- Complete assembly of 16-bit counter
- Design and build circuit for 17th bit
- Test address generator
- Measure time delay of 2 AND gates
- Can move on to the next step
- Build RAM read/write control circuit
- Test RAM read/write control circuit
Project Circuit
This Week

[Diagram showing an electronic circuit with components ADC, RAM, DAC, Address Gen, R/W Control, and Clock, with connections and signal paths indicated.]
Problem: Rco_ is lagging by one clock cycle

Counter 1
A0-A7
FD=253 FE=254 FF=255 0 1

Counter 2
A8-A15
0 0 1 1 1

Combined Counter 1 & 2
A0-A15
253 254 511 256 257
Problem and Solution

Problem: RCO_ goes low earlier than expected

Solution:

Flip-Flop U11A delays the RCO_ signal by one clock pulse, counter 2 is +ve edge triggered and therefore will triggered at the end of the last count for counter 1. The delayed RCO_ signal is used to trigger the counter register clock, RCK, while the inversion of RCO_ is used to trigger the counter clock, CCK. CCK is triggered earlier than RCK. This makes sure that the output of counter 2 would be available when counter 1 resets. Notice U11A is initialized to zero, Q=0, RCO goes to the J input and RCO_ goes to the k input to avoid undesired transitions.

To generate the 17th bit, RCO_2 is delayed by one master clock pulse using U12A and is used to trigger the JK flip flop U12B. Notice that because the RCK and the CCK of counter 2 are triggered separately with a delay of one master clock cycle, RCO_2 need to be delayed by only one master clock cycle and not one cycle of counter 2 clock. The output Q, which is the inverted version of RCO_2 or RCO2 is used to trigger U12B which toggles @ every falling edge of RCO2, which is the rising edge of RCO_2, thus generating the 17th bit.
Counter 2 CCK is triggered here

Counter 2 RCK is triggered here

Delayed RCO

Delayed RCO

FD=253

FE=254

FF=255

0

1

Counter 1
Delayed Rco_1

Counter 2 CCK is triggered here

Counter 2

254 255 0

Rco_2

Delayed Rco_2

Master clock cycle

U12B is triggered here

Bit 17
17th bit switching to 1 after half the count = 2^{16} - 1 = 65535, counter 1 and 2 are reset.

RCO_2 delayed by one master clock cycle and inverted used to trigger U12B to generate the 17th bit.
**Simulation Results**

17th bit switching to 0 after 1 full cycle of counting. the count=0 to \((2^{17}-1)=0-131071\) counter 1 and 2 are reset.

RCO_2 delayed by one master clock cycle and inverted used to trigger U12B to generate the 17th bit.
Solution 2 Using the Most Significant Bit Instead of RCO

- Bit #8, B7 of counter 1, is used to trigger counter 2
- Bit #8 of counter 2, B15, is used to generate the 17th bit, B16
- The CCK is triggered earlier than RCK to make sure that counter 2 has the right count available at the output when B7 goes from 1 to zero.
Counter 2 CCK is triggered here

Counter 2 RCK is triggered here

Counter 1

B7

Counter 2

B15

17th bit B16

Counter 2 CCK is triggered here

Counter 2 RCK is triggered here

Counter 1

B7

Counter 2

B15

17th bit B16
DATA ACQUISITION CIRCUIT

OFFTIME = 31.25μs
ONTIME = 31.25μs
DELAY = 0
STARTVAL = 0
OPPVAL = 1

VOFF = 5V
FREQ = 0.5kHz
VAMPL = 5V

ECE-L304 Lecture 7
RAM Read/Write Control

End of count indicator: RCO from Address Generator or 17th bit. Each Tc clock cycle, the output toggles, switching from read to write cycle or vice-versa.

Tc = Terminal Count

should connect to ADC WR signal

U7A
74LS08

U6A
74LS107A

Delayed Clock
RE = Read Enable
OE = Output Enable
WE = Write Enable
All are active HIGH

Write cycle
Read cycle
## RAM Read/Write Control

<table>
<thead>
<tr>
<th>CE1_</th>
<th>CE2</th>
<th>OE_</th>
<th>WE_</th>
<th>Mode</th>
<th>I/O</th>
<th>Supply Current</th>
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<tbody>
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<td>X</td>
<td>X</td>
<td>X</td>
<td>Not Selected</td>
<td>High Impedance</td>
<td>I$SB$</td>
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<tr>
<td>X</td>
<td>L</td>
<td>X</td>
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<td></td>
<td>High Impedance</td>
<td>ICCA</td>
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<tr>
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<td>H</td>
<td>H</td>
<td>H</td>
<td>Output Disable</td>
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<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>DOUT</td>
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</tr>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>Write</td>
<td>DIN</td>
<td></td>
</tr>
</tbody>
</table>

$X$ = don’t care  
$I_{CCA}$ is operating supply current, $I_{SB}$ is standby supply current
RAM: WE_ Controlled Write

Address (Input)

CE1 (Input)

CE2 (Input)

WE (Input)

I/O (Input/Output)

Indefinite data out

High impedance

Data in

High impedance

Indefinite data out
RAM: CE1 Controlled Write

[Diagram showing the timing signals for CE1, Address, CE2, WE, and I/O with labels for t_{AS}, t_{CW1}, t_{CW2}, t_{AW}, t_{WP}, t_{WR}, t_{DW}, and t_{DH}.]
RAM :CE2 Controlled Write
Read Cycle Timing

Diagram showing the timing of the read cycle with various timing parameters labeled.
Step 6 Prelab Task

- Judge whether the JKFF/AND gate circuit from Step 4 is suitable for our purposes
- Will this circuit properly control the NEC RAM chip?
- **Redesign** the control to operate the active-low inputs of the RAM chip
- AND gates, JKFFs and Inverters are provided in your parts kit
Step 6

Part 1

- Assemble the 16-bit address generator
  - Place the circuitry according to your floorplan
  - Connect the LS590 outputs to the A0-A15 board center connector pins
  - Use the 555 counter to clock the LS590, not the function generator (noise)

- Design and build a circuit that will provide a 17th bit
  - This step is required to get full hardware credit

- Confirm functionality using the logic analyzer
Step 6
Cascaded 74LS590 Chips
Step 6

Part 2

Add two AND gates between clock output and counter input

This is for testing purposes only - in your circuit this delay would be between CLK and RAM WE

Observe time delay between incoming and exiting clock pulses on the logic analyzer

Calculate the delay per gate
Step 6

Part 3: part of step 7

Assemble the control circuitry you designed in the prelab

Place and wire the circuitry according to your floorplan

Connect RAM CE1 and CE2 to the proper logic levels or control circuit

Confirm functionality using the logic analyzer
Board Center Connectors

- ADC Control
  - CS_, RD_, WR_, INTR_
- Power, GND
- RAM Control
  - CE1_, CE2, OE_, WE_
- RAM Addresses
  - A16 - A0
Step 6 Deliverables

- **Hardware**
  - Have functionality of address generator and control circuit checked by TA

- **Report**
  - Introduction
  - Part 1: A verified 17-bit address generator
    - Include in your report well labeled screen capture(s) from the scope/logic analyzer that verify the functionality
Step 6 Deliverables

- **Report (cont)**
  - **Part 2: Results of AND gate delay test**
    - What is the delay per gate?
    - Document with a screen capture
  - **Conclusions**
    - Comment on your observations
Start building an overall system timing diagram. Indicate with arrows which signal edge controls the function. For example, control FF uses falling edge, while 590 counter uses rising edge.