STEP 6. BUILD AND TEST THE ADDRESS GENERATOR

PRELAB

Read the data sheets for the 74LS112 Dual JK Flip Flop, 74LS08 Quad AND gate, and 74LS590 8-bit counter.

TASKS

PART I BUILD ADDRESS GENERATOR

• Assemble a 16 bit address generator using two 74LS590 8-bit counters. To get full credit for your hardware, design a simple modification to create a 17th bit. The memory chip will require all 17 bits to get the full use of the 128 KB available and to maximize the record time.

• The first counter takes the output of the 555 timer on board, the register clock RCLK and the counter clock CCLK may be tied together. G and CCLKEN should be connected to ground. CCLR should be connected to VCC. Connect the output of the first counter QA to QH to the lowest RAM addresses A0 to A7 in the center of your board. Observe A0 to A7 on the logic analyzer and confirm functionality. This counter should count from 0 to 255. Observe RCO_ of this counter on one of the logic analyzer probes, save a screen capture having RCO_ and A7, notice when RCO_ goes low.

• Design a circuit that would hold the RCO_ signal of counter 1 for one clock cycle, use the delayed RCO_ to drive the second counter or think of any other circuit that can fix the timing error, or signals other than Rco_ that can trigger the second counter.
• For counter 2, the register clock RCLK and the counter clock CCLK may be tied together. G and CCLKEN should be connected to ground. CCLR should be connected to VCC. The output of counter 2, QA to QH, should connect to address lines A8 to A15 in the center of your board.

• Observe the address generator outputs A0-A15 on the logic analyzer and confirm functionality. Try to find the transition from decimal count 65536 ($2^{16}$) to 0.

• Design a circuit that would hold the RCO_ signal of counter 2 for 1 clock cycle, notice that the clock cycle of counter 2 is one cycle of the delayed RCO_ signal of counter 1, which is 256 times the clock cycle of counter 1.

• Use the delayed RCO_ of counter # 2 or other possible signals to create the 17th bit. This bit should go to A16 of the RAM address in the center of your board.

• To observe the 17th bit, since our analyzer has only 16 bits, watch the highest 16 bits on the 17-bit counter A1-A16. Save a screen capture of your analyzer result for your report.

PART II ADD TWO AND GATES

• Add two AND gates in series having the on board timer clock as an input, shown in figure 2. Each of these gates should have their inputs tied together. Observe time delay between incoming and exiting clock pulses on the logic analyzer. Calculate the delay per gate. Since the two inputs of the AND gate are tied together, the steady-state output logic level will always be equal to the steady-state input logic level. The only purpose of the gate is to introduce a small time delay between input and output.

![Diagram of AND gates](image)

**FIGURE 2**

DELIVERABLES

HARDWARE

• Have functionality of address generator checked by TA

REPORT

• Introduction

• Part 1:
  ✓ A verified 17-bit address generator
  ✓ Include in your report well labeled screen capture(s) from the scope/logic analyzer that verify the functionality.
• Part 2: Results of AND gate delay test
  ✓ What is the delay per gate?
  ✓ Document with a screen capture.
• Conclusions.
• Comment on your observations.