DATA ACQUISITION PROJECT, STEP 1

These instructions are based on Cadence PSD 14.2 tools

PRELAB

- Read "Memory Devices, Timing Models, and Hierarchical Blocks", A. Motley, MicroSim Corporation, April 1997 through the "The Supporting Logic" section.
- Review ADC, DAC experiments from ECE-L303 Lab III
- Find a box to safely carry around your circuit (6" x 8" x 3" min)

DISCRETE DAC

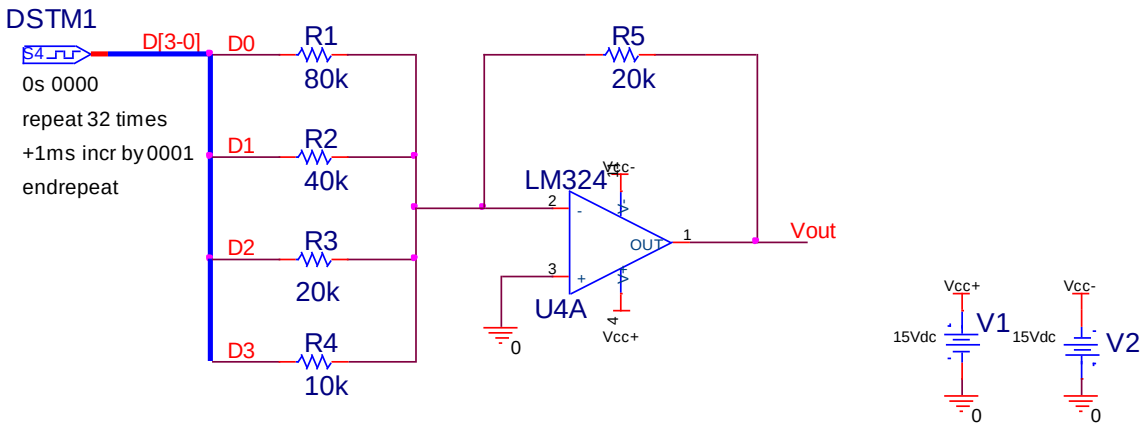

Figure 1. Discrete DAC Schematic

Components Used

Part No	Type	Description	PSpice Library
V1, V2	VDC	dc voltage source	source
U4A	LM324	opamp	opamp
Rn	R	resistor	analog
DSTIM1	Stim4	4-bit digital word generator	source

1. Predict and graph the expected output of the Discrete DAC summing circuit for 0 ≤ time ≤ 16 ms A paper sketch is sufficient, but Excel is acceptable as well.
2. Create a new Cadence Capture CIS (Studio) project. Create this project using "Analog or Mixed A/D". Failure to do this will result in a schematic that you cannot simulate.
3. Add a schematic to your project: capture the Discrete DAC summing circuit in Capture CIS.

a. Display all DSTM1 commands, as in Figure 1.
b. Add your name(s) and section to the block in the lower right of your schematic.

4. Set up a simulation profile and simulate your circuit for 0 ≤ time ≤ 32 ms. Graph V(D0), V(D1), V(D2), V(D3), and the output voltage vs time. In the circuits that use the LM324 opamp (Discrete DAC and Discrete ADC) you may have a convergence error in the transient simulation. You can solve this problem by forcing PSpice to take smaller time steps in its solution. Try setting the minimum time step to about 10us in the transient simulation profile. If you still have trouble, reduce this time until the simulation succeeds.
5. Determine the value of a feedback resistor that will produce an output of -5 V for an input of 0101_2. Verify your design by simulating the new circuit.

DISCRETE ADC CIRCUIT

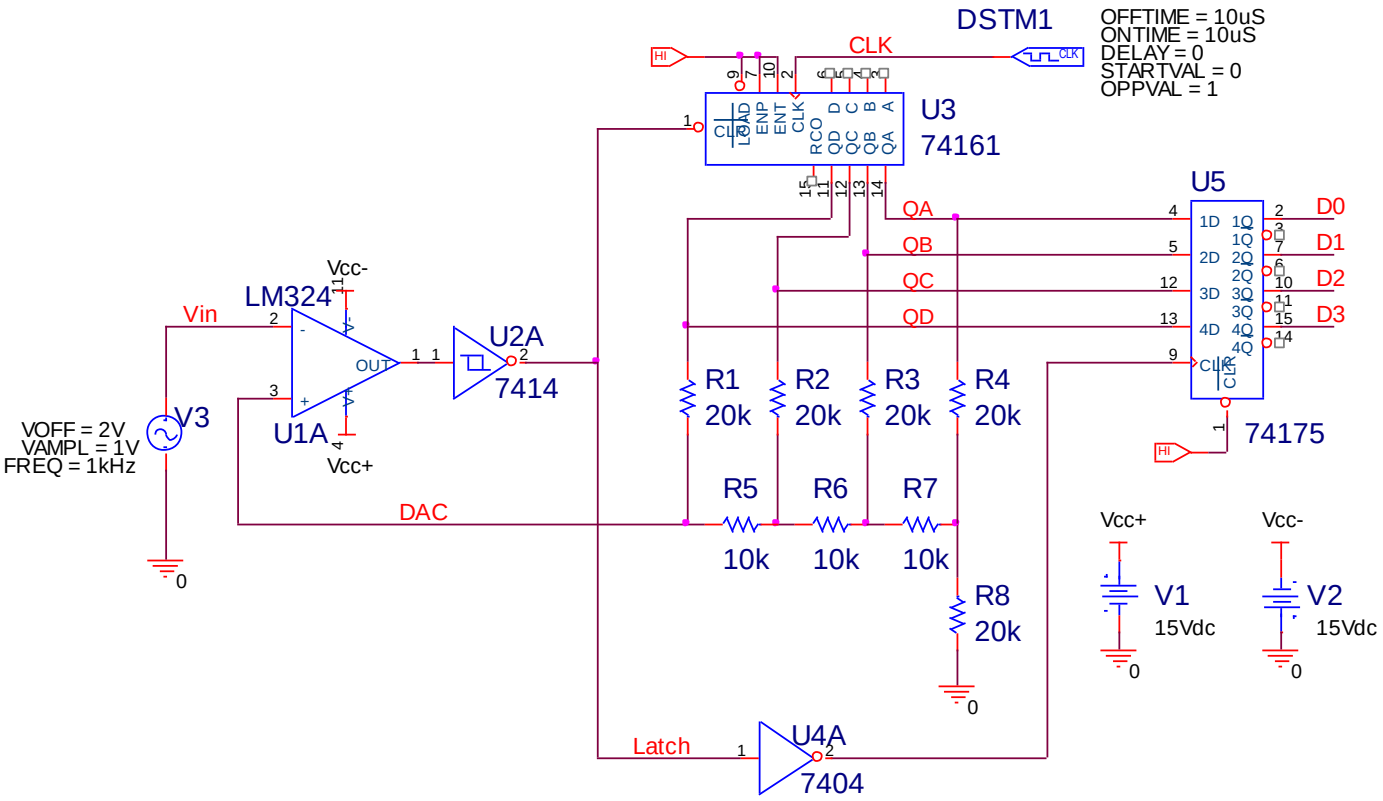

Figure 2. Discrete ADC Schematic

Components Used:

Part No	Type	Description	PSpice Library
V1, V2	VDC	dc voltage source	source
V3	VSIN	sine generator	source
U1A	LM324	opamp	opamp
U2A	7414	inverting Schmitt trigger	7400
Rn	R	resistor	analog
U3	74161	binary counter	7400
U5	74175	D flip flop	7400
DSTIM1	DigClock	clock	source
HI	HI	digital high	source (use Place Power tool)

6. Add a new schematic to your project: capture the Discrete ADC circuit of Figure 2. The instructions for creating the schematic are given below:
    a. Return to your Project window
    b. Right click in the Design icon
        i. Choose New Schematic and give the schematic a name
    c. Right click in the Schematic directory icon you just created
        i. Choose New Page
    d. Save your Project – the Project window must be in front
    e. Right click in the Schematic directory icon you created
        i. Choose Make Root, making this schematic the one to be simulated
    f. Double click on the schematic page icon to begin your design
7. Make sure the Discrete ADC schematic is "root", and simulate the circuit for 0 ≤ time ≤ 2 ms. Graph Clk, D3 – D0, Latch, Vin, and DAC vs time for 0 ≤ time ≤ 2 ms
    a. Simulations of circuits that use components with internal flip-flops (74161, 74175) should initialize those flip-flops to get best results. In the Options tab of the Simulation Settings, choose Category: Gate-level Simulation, and initialize all flip-flops to 0.
    b. You can graph a bus by grouping the binary bits from most significant to least significant within curly brackets. If a bus has bits A7 – A0, you can plot the bus A by adding the trace {A7 A6 A5 A4 A3 A2 A1 A0};A;D or {A[7:0]}. The signal will be shown as trace "A" with decimal (D) values. If the ;D had been omitted, the trace would be shown in hex (default). If the bits are to be traced individually, adding the trace, A[7:0] will add seven individual traces for the bits A7 to A0.

INTEGRATED CIRCUIT ADC/DAC

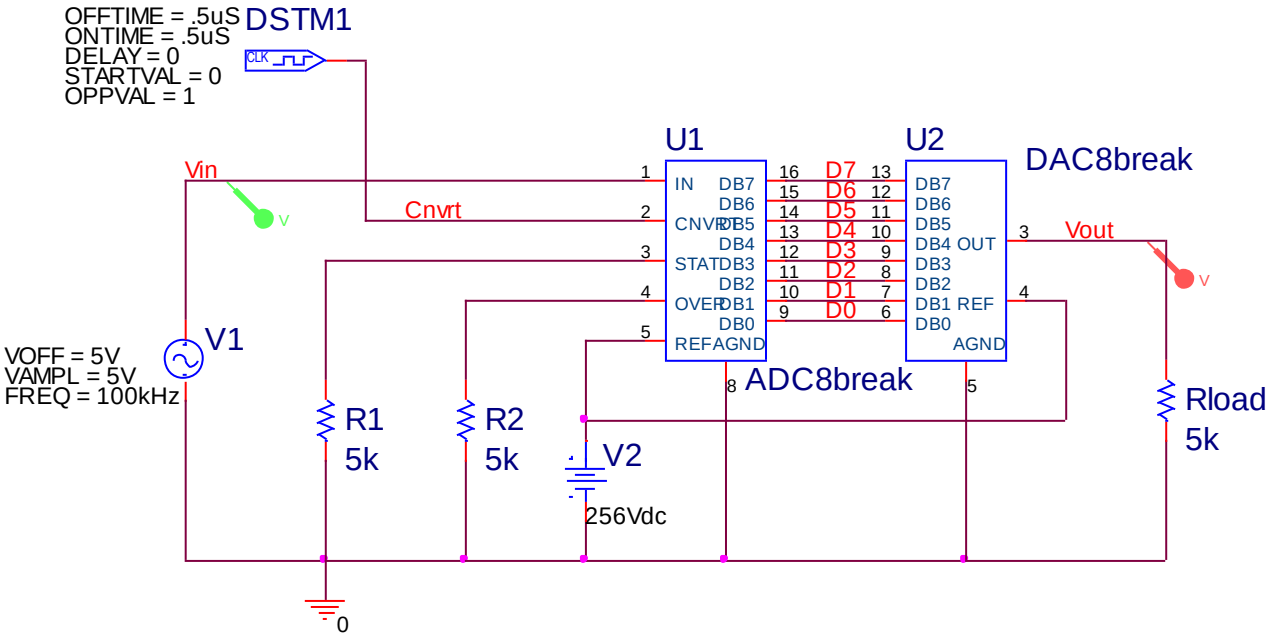

Figure 3. Integrated ADC/DAC

Components Used:

Part No	Type	Description	PSpice Library
V1	VSIN	sine generator	source
V2	VDC	dc voltage source	source
U1	ADC8break	8-bit ADC	breakout
U2	DAC8break	8-bit DAC	breakout
Rn	R	resistor	analog
DSTIM1	DigClock	clock	source

8. Add a new schematic to your project and capture the Integrated Circuit ADC circuit of Figure 3. Follow the same instructions above to create the new schematic.
9. Make sure the new circuit is the root schematic and simulate your circuit for 0 ≤ time ≤ 20 us. Graph D7 – D0, Cnvrt, Vin, and Vout vs time for 0 ≤ time ≤ 20 us.
    a. Note the voltage and time resolution

The value of the DAC output is

$$V_{out} = V_{ref}\left[\frac{D7}{2}+\frac{D6}{4}+\frac{D5}{8}+\frac{D4}{16}+\frac{D3}{32}+\frac{D2}{64}+\frac{D1}{128}+\frac{D0}{256}\right]$$

where the values of the DAC input (D7-D0) can be 1 or 0

10. Recalibrate this circuit (adjust the reference voltage) to produce the maximum analog output of 10V when the input to the DAC is 11111111_2. Show your work. (Since 11111111_2 = 255, your solution should be slightly larger than 10V.)
11. Change the reference voltage to your calculated value, and increase the clock frequency to 10 MHz. Compare the voltage and time resolution to the previous case.

STEP 1 DELIVERABLES

- Introduction to Step 1
  - 1 – 2 paragraphs
- Graph of prediction of Discrete DAC performance.
- Discrete DAC schematic and simulation results.
- Calculation of new feedback resistor for Discrete DAC.
- Simulation results for Discrete DAC with new feedback resistor.
- Short discussion of Discrete DAC results.
- Discrete ADC schematic and simulation results.
- Short discussion of Discrete ADC results.
- Integrated Circuit ADC/DAC schematic and simulation results for 256 V reference voltage, 1 MHz clock, circuit voltage and time resolution.
- Integrated Circuit ADC/DAC schematic and simulation results for recalibrated reference voltage, 10 MHz clock, circuit voltage and time resolution.
- Short discussion of Integrated Circuit ADC/DAC results, including comments on voltage and time resolution.
- Answers to discussion questions
  - The recalibrated Discrete DAC summing circuit of Part 5 fails to produce an output of 15 V for an input of 1111_2. Why? How would you correct this problem?
  - Discuss how the Discrete ADC circuit operates. Your discussion should include, at the minimum: What is the function of the R1 – R8 block? When does the Latch signal change? What functions does this signal perform? Why is U5 necessary? What is the relationship between input voltage and conversion time?
- Conclusions

These assignments are based on material in "OrCAD PSpice for Windows, Volume III: Digital and Data Communications, 3rd ed.", R.W. Goody, Prentice Hall, 2001.