STEP 4 INSTRUCTIONS

PURPOSE

- Introduce the static RAM chip
- Write mode, read mode
- Introduce the address generator
- Step the address from 00H to FFH (256 steps) using 8 bits
- "H" indicates hexadecimal format
- Introduce control
- Record 256 words in RAM, then play back

ACTIVITIES

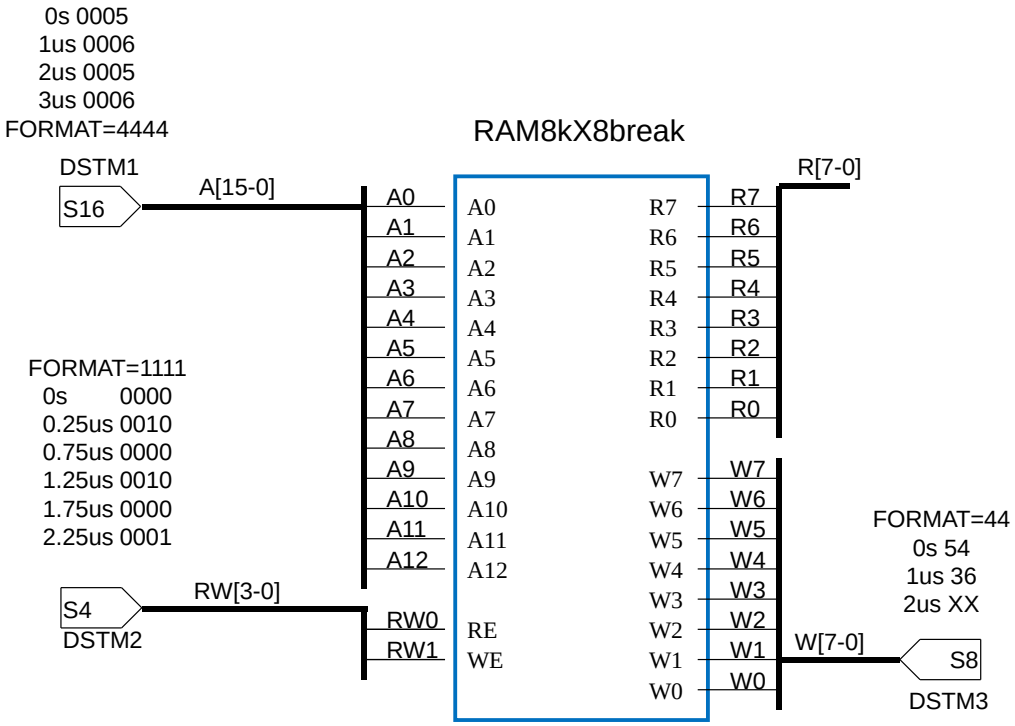
PART 1 GOALS

- Write two data bits to two RAM locations and read them back
- Learn to display data in hex format in Probe
- Observe Read/Write operations and timing
- Generate Part 1 schematic in OrCAD
- Show through simulation that the circuit performs the following activities:
  - Write data 54H from port W to address 5H
  - Write data 36H from port W to address 6H
  - Read the contents of address 5H to port R
  - Read the contents of address 6H to port R

PARTS USED

PART NO	TYPE	DESCRIPTION	PSPICE LIBRARY
DSTIM1	Stim16	16-bit digital word generator	source
DSTIM2	Stim4	4-bit digital word generator	source
DSTIM3	Stim8	8-bit digital word generator	source
U5	RAM8Kx8break	8Kx8 RAM	breakout

Part 1 Schematic - Read/Write Exercise



Part 1 Schematic

Part 2 Goals

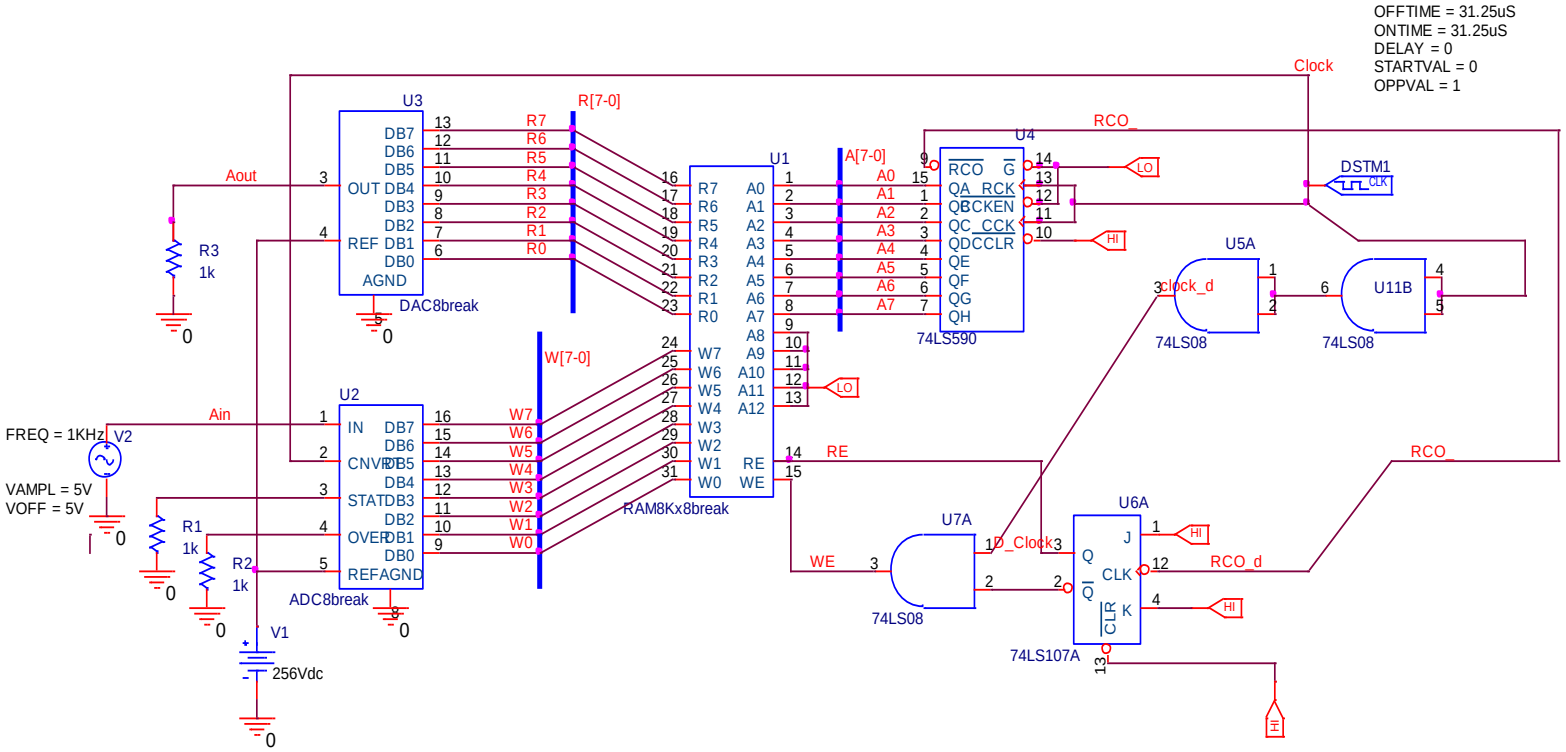
- Write 8-bit ADC data to 256 locations and read it back
- Generate Part 2 schematic in OrCAD
- Simulate the following activities
  - Write 8-bit ADC data to the lowest 256 addresses in memory
  - Read the lowest 256 addresses to the R port
  - Generate an analog signal using these 8-bit word

Parts Used

Part No	Type	Description	PSpice Library
V1	VDC	dc voltage source	source
V2	VSIN	sine generator	source
Rn	R	resistor	analog
U5	RAM8Kx8break	8Kx8 RAM	breakout
U10	ADC8break	8-bit ADC	breakout
U11	DAC8break	8-bit DAC	breakout
U7A	74LS08	AND Gate	74LS
U8A	74LS08	AND Gate	74LS
U12A	74LS08	AND Gate	74LS
U9	74LS590	8 bit binary counter	74LS

U6A	74LS107A	JK flip flop	74LS
DSTIM1	DigClock	clock	source
HI	HI	digital high	source (use Place Power tool)
LO	LO	digital Low	source (use Place Power tool)

Part 2 Schematic - Data Acquisition Exercise



Step 4 Deliverables

Complete Part 1 Simulation

- Part 1 Schematic
- Part 1 Simulation
- Plot A[15-0], W[7-0], RW1, RW0, R[7-0] vs time over span of 0 to 4 us
- Are proper read/write timing rules followed?
- Relationships between address, data, RE, WE
- Is the data read from memory identical to what was written?

Complete Part 2 Simulation

- Part 2 Schematic
- Part 2 Simulation
- Plot W[7-0], R[7-0], WE, RE, RCO_, AIN, AOUT vs time over one complete read/write cycle. Hint: The duration of one read or write cycle equals clock_cycle*256.

- Are proper read/write timing rules followed?
- Relationships between address, data, RE, WE
- Does the data read from memory and converted to analog (AOUT) match the input waveform (AIN) to the resolution of the system?
- What is the propagation delay through the 74LS590 counter? Hint: to find the propagation delay of the counter, which should be in the order of nanoseconds, observe the time delay between the positive edge of the clock and the transition of the least significant bit of the counter A_0. You will need to zoom in around the edge of the clock within a 1us range or less. The MicroSim library "dig_io.lib" contains the full timing parameters for its models. You can simulate using timing parameters for the minimum (MN), typical (TY), and maximum (MX) values for each device. PSpice provides the option to run all of the components in the circuit at either their MN, TY, or MX values. To setup the timing values, go to Edit Simulation Profile→ Transient Analysis → Options → Gate level Simulation→ choose Minimum, Typical or Maximum values. If a particular part or several different parts require that their timing parameters are simulated at a different level from the global setting, then these parameters can be set by double clicking the part and typing in the value of 1 for Min, 2 for Typical, or 3 for Max in the "MNTYMXDLY" attribute line.
- Why is there a lag time in the READ operation between the time RE goes high and when the data is valid?
- [Extra Credit] How would you correct the timing flaw at the transition from write to read? Repeat the simulation with the correction and include the results in your report. Hint, notice the time of the transition of the RCO_ output of the counter and the corresponding address at the transition.